AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 7, line 19 with the following amended paragraph:

The additional mirroring can be implemented as shown in **FIGS.** 6a and 6b ~~5a and 5b~~. **FIG. 6**b includes additional transistors T7-t**14**. MIRRP and MIRRN nodes come off the main mirror in **FIG. 6**a, but the ratio 1:F is chosen to be small so that devices T**7** and T**8** do not load the main mirror excessively and thereby degrade its performance. The high mirror ratio required to deliver power to the load is implemented by the PMOS current mirror consisting of devices T**9**, T**10**, T**13**, T**14** and the NMOS current mirror consisting of devices T**11**, T**12**, T**5** and T**6**. The effective mirror ratio of this "secondary" current mirror is $(F\times q/p\times D/\gamma):1$ as is evident from **FIGS.** 6a and 6b ~~5a and 5b~~. Also, even though the description has used CMOS transistors, the above ideas are by no means restricted to CMOS technology. It could be implemented in bipolar, bi-CMOS, or any other technology, including non-monolithic technology.